PVP 20

Code: 20EC4501D

III B.Tech - I Semester – Supplementary Examinations
NOVEMBER 2023

COMPUTER ARCHITECTURE & ORGANIZATION
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

			Max. Marks
UNIT-I			
1	a)	Explain the concept of register transfer in computer organization. How is data transferred between registers using register transfer notation?	7 M
	b)	Illustrate the operation of a 4-bit binary adder in register transfer notation. Provide a step-by-step explanation.	7 M
OR			
2	a)	Construct a bus system for four registers using multiplexers. Describe the components and connections involved.	7 M
	b)	Explain logic micro-operations in computer organization. Provide examples of logic micro-operations and their applications.	7 M

UNIT-II			
3	a)	Explain the significance of instruction codes in a computer's instruction set architecture (ISA).	4 M
	b)	How does a CPU determine the type of instruction during the fetch and decode phase? Outline the examples of different instruction types.	10 M
OR			
4	a)	Explain the concept of a common bus system in computer organization. How does it enable communication between different registers?	7 M
	b)	What are the key steps in the interrupt cycle? How does the CPU handle interrupts and return to the interrupted program?	7 M
UNIT-III			
5	a)	Demonstrate the concept of a Register Stack and its role in computer organization. How does it differ from a Memory Stack?	7 M
	b)	List the examples of data manipulation instructions and explain their role in performing arithmetic and logical operations.	7 M
OR			
6	a)	Define addressing modes in computer architecture. Explain the purpose of addressing modes in instruction execution.	10 M
	b)	Explain conditional branch instructions in computer organization.	4 M

UNIT-IV			
7	a)	Explain the process of addition with signed-magnitude data. Provide an example to illustrate the steps involved.	8 M
	b)	Demonstrate the concept of memory hierarchy in computer systems.	6 M
OR			
8	a)	Analyze the hardware circuitry used for signed-magnitude subtraction.	4 M
	b)	Explain the concept of address mapping in virtual memory systems. How are virtual addresses translated into physical addresses?	10 M
UNIT-V			
9	a)	Explain the purpose of an I/O bus and interface modules in connecting peripheral devices to a computer. How do these components facilitate data transfer?	7 M
	b)	Analyze the function of a DMA controller. How does it facilitate DMA transfers between memory and peripheral devices?	7 M
OR			
10	a)	Demonstrate the priority interrupt handling mechanism in computer systems.	6 M
	b)	Analyze the significance of handshaking in asynchronous data transfer. How does it ensure data integrity during I/O operations?	8 M